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EXAMINER	
BROCK II, PAUL E	

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2815	29

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/351,544	Applicant(s) CARNS ET AL.	
	Examiner Paul E Brock II	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-11,26-30,36-39 and 72-101* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-11,26-30,36-39 and 72-101* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *26 February 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The corrected or substitute drawings were received on February 26, 2002. These drawings are approved.

Claim Objections

2. Claim 81 is objected to because of the following informalities: "an anti-reflective layer" on the 9th line of the claim should be --said anti-reflective layer--. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 81 – 101 rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. With regard to claim 81, the specification does not enable one of ordinary skill in the art to optimize process parameters for forming capacitors and transistors. With regard to claim 86, the specification does not enable one of ordinary skill in the art to perform the step of optimizing parameter values of a transistor flow. With regard to claims 91 and 97, the specification does not enable one of ordinary skill in the art to optimize process parameters.

5. Claims 81 – 101 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

With regard to claims 81 – 85 it is not clear where in the originally filed specification support for "wherein the process parameters of the portions of said process flow for forming one or more transistors prior to and subsequent to said performing a capacitor process module are optimized with the capacitor process module omitted, and wherein the process parameters for the capacitor module are optimized for capacitor formation while maintaining the process parameters of said process flow for forming one or more transistors optimized with the capacitor process module omitted," can be found. Further, with specific regard to claim 83, it is not clear where in the originally filed specification support for "the thickness of said conformal insulating layer is selected to optimize the capacitor formation while maintaining the process parameters of said process flow for forming one or more transistors optimized with the capacitor process module omitted" can be found.

With regard to claims 86 – 90, it is not clear where in the originally filed specification support for "optimizing parameter values of a transistor flow to form a conductive layer, thereafter to from an anti-reflective layer on the conductive layer, and thereafter to define and etch the conductive layer using the anti-reflective layer, whereby the control gates of one or more transistor gates are formed, and wherein said etch is performed using a photoresist and said

parameter values of the transistor flow include the thickness of the photoresist," can be found. Further with regard to claims 86 – 90, it is not clear where in the originally filed specification support for "the subsequently..." clause in claim 86 can be found.

With regard to claims 91 – 96, it is not clear where in the originally filed specification support for "wherein a), b), c) and d) are performed according to a first set of process parameters including the thickness of said mask that have been optimized for said gate formation;" and "wherein said forming an insulating structure is performed according to a second set of process parameters optimized to electrically isolate said top electrode from the conductive layer while keeping said first set of process parameters the same," can be found.

With regard to claims 97 – 101, it is not clear where in the originally filed specification support for "wherein said forming... are optimized for said gate formation;" and "forming, subsequent to said forming a capacitor structure and prior to said forming a antireflective layer, an insulating structure defined by a second set of process parameters optimized for electrically isolating the top electrode from the conductive layer wile keeping first ser of process parameters the same," can be found.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 3, 8 – 11, 36, 39, 74, 81 – 83, 85, 97, 98, and 100 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi (USPAT 5683931) in view of Bencher et al. ("Dielectric Antireflective coatings for DUV Lithography", Solid State Technology, March 1997, p. 109, Bencher).

With regard to claim 3, Takahashi discloses in figures 2a – 2e forming a capacitor in an integrated circuit. Takahashi discloses in figure 2a forming a bottom electrode layer (304) on a semiconductor body (301). Takahashi discloses in figure 2b forming a dielectric layer (305) over at least a portion of the bottom electrode. Takahashi discloses in figure 2b forming a top electrode layer (306) over at least a portion of the dielectric layer. Takahashi discloses in figure 2c removing a portion of the top electrode layer to expose a portion of the dielectric layer, thereby forming a top electrode; and subsequently removing at least a portion of the exposed portion of the dielectric layer to expose a portion of the lower electrode layer, wherein a portion of the dielectric is removed from an intermediate region between the top electrode and the bottom electrode layer. Takahashi discloses in figure 2d subsequently forming a conformal insulating layer (307) over at least a portion of the exposed portion of the bottom electrode layer proximate to the exposed dielectric layer, the exposed dielectric layer and at least part of the top electrode layer proximate to the exposed dielectric layer, whereby a portion of the conformal insulating layer is formed in the intermediate region. Takahashi discloses in figure 2e etching the bottom electrode layer using a photolithographic mask (309) subsequent to forming the conformal insulating layer. Takahashi is silent to teaching forming an anti-reflective layer (ARL) over at least a portion of the conformal insulating layer. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a

photolithographic process over at least a portion of a resultant structure. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the antireflective layer of Bencher subsequent to forming the conformal insulating layer and before forming the photolithographic mask in the method of Takahashi in order to improve the photolithographic process by reducing net linewidth variations as stated by the Applicant's admitted prior art (AAPA) on page 1, lines 14 – 15 of the originally filed specification.

With regard to claim 8, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the ARL is an anti-reflective coating.

With regard to claim 9, Bencher teaches in the first paragraph after the Dielectric ARC Design section wherein the ARL is titanium nitride.

With regard to claim 10, Bencher teaches in the first sentence of the article wherein the ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

With regard to claim 11, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the plasma enhanced chemical vapor deposition anti-reflective layer has a thickness of 300 angstroms.

With regard to claim 36, Takahashi discloses in figure 2b forming a conductive layer on a semiconductor body. Takahashi discloses in figure 2c forming a capacitor structure comprising: a top electrode over a portion of the conductive layer; and a dielectric layer between the top electrode and the conductive layer. Takahashi discloses in figure 2d forming a conformal insulating layer over the capacitor structure and at least a portion of the conductive layer proximate to the capacitor structure, whereby a portion of the conformal layer is formed in the region between the top electrode and the conductive layer. Takahashi discloses in figure 2e

forming a patterned mask over the structure resultant from the forming a conformal insulating layer. Takahashi is silent to teaching forming an anti-reflective layer (ARL) over at least a portion of the resultant structure resultant from forming the conformal insulating layer before forming the patterned mask. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of a resultant structure before forming a patterned mask. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the antireflective layer of Bencher on the structure resultant from the forming the conformal insulating layer and before forming the patterned mask in the method of Takahashi in order to improve the photolithographic process by reducing net linewidth variations as stated by the Applicant's admitted prior art (AAPA) on page 1, lines 14 – 15 of the originally filed specification. Takahashi discloses in figure 2e etching the conductive layer using the patterned mask.

With regard to claim 39, Takahashi discloses in figure 2e wherein the conductive layer is additionally used to form the gate of one or more transistors formed on the integrated circuit.

With regard to claim 74, Bencher discloses in the Step 2 section under Dielectric ARC Design wherein the anti-reflective layer is a Si_xON_y film.

With regard to claim 81, Takahashi discloses in figures 2a – 2f a method of forming an integrated circuit. Takahashi discloses in figure 2a forming a conductive layer (304) on a semiconductor body. Takahashi discloses in figure 2e subsequently forming a patterned mask (309). Takahashi is silent to teaching forming an anti-reflective layer (ARL) over at least a portion of the resultant structure resultant from forming the conformal insulating layer before

forming the patterned mask. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of a resultant structure before forming a patterned mask. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the antireflective layer of Bencher on the structure resultant from the forming the conformal insulating layer and before forming the patterned mask in the method of Takahashi in order to improve the photolithographic process by reducing net linewidth variations as stated by the Applicant's admitted prior art (AAPA) on page 1, lines 14 – 15 of the originally filed specification. Takahashi discloses in figure 2e defining and etching the conductive layer using the patterned mask. It would have been further obvious in the method of Takahashi and Bencher that the defining and patterning would be accomplished using the anti-reflective layer, because the anti-reflective layer is used in the formation of the patterned mask. Takahashi and Bencher disclose in figures 2b – 2f of Takahashi performing a capacitor process module subsequent to said forming a conductive layer and prior to said forming the anti-reflective layer. Takahashi discloses in figures 2a – 2c forming a top capacitor electrode (306) over a portion of said conductive layer. Takahashi discloses in figures 2a – 2c forming a capacitor dielectric (305) between said top electrode and said conductive layer. Takahashi discloses in figures 2a – 2c wherein said defining and etching the conductive layer forms the gate of one or more transistors and a bottom capacitor electrode. As far as the examiner can ascertain Takahashi discloses in figures 2a – 2c wherein the process parameters of the portions of said process flow for forming one or more transistors prior to and subsequent to said performing a capacitor process module are optimized with the capacitor process module omitted, and wherein the process parameters for

the capacitor module are optimized for capacitor formation while maintaining the process parameters of said process flow for forming one or more transistors optimized with the capacitor process module omitted.

With regard to claim 82, Takahashi discloses in figures 2a – 2c forming a dielectric layer over at least a portion said conductive layer. Takahashi discloses in figures 2a – 2c forming a top electrode layer over at least a portion of said conductive layer. Takahashi discloses in figures 2a – 2c removing a portion of said top electrode layer to expose a portion of the dielectric layer, thereby forming said top capacitor electrode. Takahashi discloses in figures 2a – 2c removing at least a portion of said exposed portion of the dielectric layer to expose a portion of said conductive layer, thereby forming said capacitor dielectric between said top electrode and said conductive layer. Takahashi discloses in figures 2a – 2d forming a conformal insulating layer (307) over the structure resultant from said removing at least a portion of said exposed portion of the dielectric layer.

With regard to claim 83, as far as the examiner can ascertain Takahashi discloses in figures 2a – 2f wherein the thickness of said conformal insulating layer is selected to optimize the capacitor formation while maintaining the process parameters of said process flow for forming one or more transistors optimized with the capacitor process module omitted.

With regard to claim 85, the combination of Takahashi and Bencher teaches wherein said defining and etching the conductive layer using the anti-reflective layer comprises: forming the anti-reflective layer over the conductive layer, the top capacitor electrode and the dielectric layer between said top electrode and said conductive layer; forming a patterned mask over the anti-reflective layer; and etching said conductive layer using said patterned mask.

With regard to claim 97, Takahashi discloses in figures 2a – 2d performing a first fabrication process on a first semiconductor body (301 to the left of 302). Takahashi discloses in figures 2a – 2d forming a conducting layer (304) on the first semiconductor body. Takahashi discloses in figures 2a – 2d forming an patterned photoresist layer (309) over the conductive layer. Takahashi is silent to forming an antireflective layer over before forming the photoresist. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process before forming a patterned mask. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the antireflective layer of Bencher on the conductive layer before forming the photoresist layer in the method of Takahashi in order to improve the photolithographic process by reducing net linewidth variations as stated by the Applicant's admitted prior art (AAPA) on page 1, lines 14 – 15 of the originally filed specification. It would be further obvious in the method of Takahashi and Bencher that the patterned photoresist layer is formed over the antireflective layer. Takahashi discloses in figures 2a – 2d etching the conductive layer using said patterned photoresist layer into gates for one or more transistors. It is further obvious in the method of Takahashi and Bencher that wherein said forming a conducting layer, forming an antireflective layer, forming a patterned photoresist layer, and etching the conductive layer in the first fabrication process on the first semiconductor body are defined by a first set of process parameters including the thickness of said photoresist that are optimized for said gate formation. Takahashi discloses in figures 2a – 2d performing a second fabrication process on a second semiconductor body (301 below 302). Takahashi discloses in figures 2a – 2d forming a second conducting layer (304) on the second semiconductor body. Takahashi discloses in figures 2a – 2d

forming a capacitor structure including a top electrode (306) over a portion of the second conductive layer and an inter-electrode (305) therebetween. The combination of Takahashi and Bencher teach forming an antireflective layer over the second conductive layer and the capacitor structure. The combination of Takahashi and Bencher teach forming a patterned photoresist layer (309) over the second antireflective layer. Takahashi discloses in figures 2a – 2d etching the conductive layer using said patterned photoresist layer, thereby forming a lower capacitor electrode for the capacitor structure. It is further obvious in the method of Takahashi and Bencher wherein said forming a conducting layer, forming a antireflective layer, forming a patterned photoresist layer, and etching the conductive layer in the second fabrication process on the second semiconductor body are defined by said first set of process parameters. It is further obvious in the method of Takahashi and Bencher forming, subsequent to said forming a capacitor structure and prior to said forming a antireflective layer, an insulating structure (307) defined by a second set of process parameters optimized for electrically isolating the top electrode from the conductive layer while keeping first set of process parameters the same.

With regard to claim 98, Takahashi discloses in figures 2a – 2d wherein said forming an insulating structure comprises: forming a conformal dielectric layer formed over said capacitor structure and said conductive layer, wherein the second set of process parameters includes a thickness for said conformal dielectric layer.

With regard to claim 100, Takahashi discloses in figures 2a – 2d, including the anti-reflective layer teaching of Bencher, wherein the first set of process parameters further includes the thickness of said antireflective layer.

8. Claims 4 – 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi in view of Bencher and Wang et al. (USPAT 5545585, Wang).

With regard to claim 4, Takahashi discloses in figures 2a – 2e forming a capacitor in an integrated circuit. Takahashi discloses in figure 2a forming a bottom electrode layer (304) on a semiconductor body (301). Takahashi discloses in figure 2b forming a dielectric layer (305) over at least a portion of the bottom electrode. Takahashi discloses in figure 2b forming a top electrode layer (306) over at least a portion of the dielectric layer. Takahashi discloses in figure 2c removing a portion of the top electrode layer to expose a portion of the dielectric layer, thereby forming a top electrode; and subsequently removing at least a portion of the exposed portion of the dielectric layer to expose a portion of the lower electrode, wherein a portion of the dielectric layer is removed from an intermediate region between the top electrode and the bottom electrode layer. Takahashi discloses in figure 2d subsequently forming a conformal insulating layer (307) over at least a portion of the exposed portion of the bottom electrode layer proximate to the exposed dielectric layer, the exposed dielectric layer and at least part of the top electrode layer proximate to the exposed dielectric layer, whereby a portion of the conformal insulating layer is formed in the intermediate region. Takahashi discloses in figure 2e etching the bottom electrode layer using a photolithographic mask (309) subsequent to forming the conformal insulating layer. Takahashi is silent to teaching forming an anti-reflective layer (ARL) over at least a portion of the conformal insulating layer. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of a resultant structure. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the

antireflective layer of Bencher subsequent to forming the conformal insulating layer and before forming the photolithographic mask in the method of Takahashi in order to easily maintain critical dimension (CD) control during pattern transfer in a photolithographic step as stated by Bencher in the last paragraph before the Dielectric ARC Design section. Takahashi and Bencher are silent to the conformal insulating layer having a thickness in the range of from 20 Å to 70 Å. Wang discloses in figure 7, column 7, lines 65 – 67 and column 8, lines 1 – 16 a conformal insulating layer (42) that has a thickness of 45 Å. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of the conformal insulating layer of Wang in the method of Takahashi and Bencher in order to form a material of high dielectric constant that is compatible with ULSI polysilicon processing as stated by Wang in column 1, lines 16 – 17, column 7, lines 65 – 67 and column 8, lines 1 – 16.

With regard to claim 5, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the conformal insulating layer is an oxide layer is formed in a thermal process.

With regard to claim 6, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the thermal process is a thermal oxidation. Takahashi, Bencher and Wang do not disclose that the conformal insulating layer is formed in a rapid thermal process that is a rapid thermal oxidation performed for a length of time in the range of from 10 to 60 seconds and at a temperature in the range from 850°C the 1050°C. It is well known in the art to use a rapid thermal process in the production of a thermal oxide layer that has parameters of from 10 to 60 seconds and at a temperature in the range from 850°C the 1050°C. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use a rapid thermal process that has parameters of from 10 to 60 seconds and at a temperature in the range from

850°C the 1050°C to form the conformal insulating layer of Takahashi, Bencher and Wang in order to choose a method that is widely used and understood in the art and produces a consistent and reliable oxide layer.

With regard to claim 7, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the conformal insulating layer is formed by deposition.

9. Claims 26 – 30, 80, 86, 87, 89, 91, 92, 93, and 95 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kayanuma in view of Bencher.

With regard to claim 26, Kayanuma discloses in figures 4d – 4e a method of forming a capacitor in an integrated circuit. Kayanuma discloses in figures 4d – 4e forming a bottom electrode layer (52) on a semiconductor body (50). Kayanuma discloses in figures 4d – 4e forming a dielectric layer (53) over at least a portion of the bottom electrode. Kayanuma discloses in figures 4d – 4e forming a top electrode layer (54) over at least a portion of the dielectric layer. Kayanuma discloses in figure 4b removing a portion of the top electrode layer to expose a portion of the dielectric layer thereby forming a top electrode, wherein the bottom electrode layer is not exposed. Kayanuma discloses in figures 4d – 4e subsequently forming a photolithographic mask (60) and removing a portion of the exposed portion of the dielectric layer and a portion of the bottom electrode layer, thereby exposing at least a portion of the semiconductor body and forming one or more capacitors. Kayanuma is silent to forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of the top electrode and the exposed portion of the dielectric layer before the step of forming the photolithographic mask. Bencher teaches in the last paragraph before the Dielectric ARC Design

section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of a resultant structure. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the antireflective layer of Bencher before forming the photolithographic mask in the method of Kayanuma in order to easily maintain critical dimension (CD) control during pattern transfer in a photolithographic step as stated by Bencher in the last paragraph before the Dielectric ARC Design section.

With regard to claim 27, Bencher teaches in the last paragraph before the Dielectric ARC Design section wherein the ARL is an anti-reflective coating.

With regard to claim 28, Bencher teaches in the first paragraph after the Dielectric ARC Design section wherein the ARL is titanium nitride.

With regard to claim 29, Bencher teaches in the first sentence of the article wherein the ARL is a plasma enhanced chemical vapor deposition anti-reflective layer (PEARL).

With regard to claim 30, Kayanuma discloses in figures 4d – 4e wherein the bottom electrode layer is additionally used to form the gate of one or more transistors formed on the integrated circuit.

With regard to claim 80, Bencher discloses in the Step 2 section under Dielectric ARC Design wherein the anti-reflective layer is a Si_xON_y film.

With regard to claim 86, Kayanuma discloses in figures 4a – 4f a method. As far as the examiner can ascertain Kayanuma discloses in figures 4a – 4f defining a CMOS process flow. As far as the examiner can ascertain Kayanuma discloses in figures 4a – 4f optimizing parameter values of a transistor flow to form a conductive layer (52). Kayanuma discloses in figures 4e thereafter to form an photoresist layer (60) on the conductive layer. Kayanuma is silent to

teaching forming an anti-reflective layer (ARL) before forming the photoresist layer. Bencher teaches in the last paragraph before the Dielectric ARC Design section thereafter to form an anti-reflective layer (ARL) before forming a photoresist layer. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the antireflective layer of Bencher before forming the photoresist in the method of Kayanuma in order to improve the photolithographic process by reducing net linewidth variations as stated by the Applicant's admitted prior art (AAPA) on page 1, lines 14 – 15 of the originally filed specification. As far as the examiner can ascertain Kayanuma discloses in figure 4e, including the anti-reflective layer teaching of Bencher, thereafter to define and etch the conductive layer using the anti-reflective layer, whereby the control gates of one or more transistor gates are formed, and wherein said etch is performed using a photoresist and said parameter values of the transistor flow include the thickness of the photoresist. As far as the examiner can ascertain Kayanuma discloses in figures 4a – 4f, including the anti-reflective layer teaching of Bencher, subsequently defining parameter values for a capacitor module to form a capacitor structure comprising a top electrode (54) over a portion of said conductive layer and a capacitor dielectric (53) therebetween and thereafter to form an insulating structure (57), wherein said defining and etching the conductive layer using the anti-reflective layer additionally forms a bottom electrode for said capacitor structure, and wherein the parameter values for the insulating structure of the capacitor module are optimized to electrically isolate the top electrode from the bottom electrode without changing the previously optimized parameter values of said transistor flow. As far as the examiner can ascertain Kayanuma discloses in figures 4a – 4f forming an integrated circuit including one or more capacitors according to said CMOS process flow.

With regard to claim 87, Kayanuma discloses in figures 4a – 4f wherein said insulating structure includes a conformal dielectric layer (57) formed over said capacitor structure, wherein said parameter values for the insulating structure of the capacitor module includes a thickness for said conformal dielectric layer.

With regard to claim 89, Kayanuma discloses in figures 4a – 4f, including the anti-reflective layer teaching of Bencher, wherein the said parameter values of the transistor flow further include thickness of said antireflective a layer.

With regard to claim 91, Kayanuma discloses in figures 4a – 4f method of forming an integrated circuit, in a first sector and a second sector. Kayanuma discloses in figures 4a – 4f forming a conductive layer (52) on a semiconductor body. Kayanuma discloses in figures 4a – 4f forming a patterned mask (60) over the conductive layer. Kayanuma is silent to teaching forming an anti-reflective layer (ARL) over the conductive layer. Bencher teaches in the last paragraph before the Dielectric ARC Design section forming an anti-reflective layer (ARL) for use in a photolithographic process over at least a portion of a resultant structure before forming a patterned mask. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the antireflective layer of Bencher on the structure resultant from the forming the conformal insulating layer and before forming the patterned mask in the method of Kayanuma in order to improve the photolithographic process by reducing net linewidth variations as stated by the Applicant's admitted prior art (AAPA) on page 1, lines 14 – 15 of the originally filed specification. Therefore, it would have been further obvious in the method of Kayanuma and Bencher to form an anti-reflective layer over the conductive layer, and form a patterned mask over the anti-reflective layer. As far as the examiner can ascertain, Kayanuma

discloses in figures 4a – 4f etching the conductive layer using the patterned mask, thereby forming the gate of one or more transistors in the first sector, wherein the above forming steps are performed according to a first set of process parameters including the thickness of said mask that have been optimized for said gate formation. Kayanuma discloses in figures 4a – 4f the method further comprising, in said second sector, performing a process prior to said forming an anti-reflective layer. Kayanuma discloses in figures 4a – 4f forming a capacitor structure including a top electrode (54) over a portion of said conductive layer and a capacitor dielectric (53) therebetween, wherein said etching additionally forms a bottom capacitor electrode in the second sector. Kayanuma discloses in figures 4a – 4f forming an insulating structure (57) over the capacitor structure. As far as the examiner can ascertain Kayanuma discloses in figures 4a – 4f wherein said forming an insulating structure is performed according to a second set of process parameters optimized to electrically isolate said top electrode from the conductive layer while keeping said first set of process parameters the same.

With regard to claim 92, Kayanuma discloses in figures 4a – 4f wherein said forming an insulating structure comprises forming a conformal dielectric layer over said capacitor structure and said conductive layer, wherein the second set of process parameters includes a thickness for said conformal dielectric layer.

With regard to claim 93, Kayanuma discloses in figures 4a – 4f wherein the method is for a CMOS fabrication process.

With regard to claim 95, Kayanuma discloses in figures 4a – 4f , including the anti-reflective layer teaching of Bencher, wherein the first set of process parameters further includes the thickness of said antireflective layer.

10. Claims 37, 38 and 84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahasi and Bencher as applied to claims 36, 40, 48, 81 and 82 above, and further in view of Wang.

With regard to claims 37 and 84, Takahashi and Bencher do not disclose that the conformal insulating layer has a thickness in the range of from 20 Å to 70 Å. Wang discloses in figure 7, column 7, lines 65 – 67 and column 8, lines 1 – 16 a conformal insulating layer (42) that has a thickness of 45 Å. It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the thickness of the conformal insulating layer of Wang in the method of Takahasi and Bencher in order to form a material of high dielectric constant that is compatible with polysilicon processing as stated by Wang in column 7, lines 65 – 67 and column 8, lines 1 – 16.

With regard to claim 38, Wang discloses in column 7, lines 65 – 67 and column 8, lines 1 – 16 wherein the conformal insulating layer is an oxide layer is formed in a thermal process.

11. Claims 72, 73 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi and Bencher as applied to claim 3 above, and further in view of the applicant's admitted prior art (AAPA).

With regard to claim 72, Takahashi and Bencher teach forming a photoresist over at least a portion of the anti-reflective layer. Takahashi and Bencher teach irradiating the photoresist. It is not clear if Takahashi and Bencher teach wherein the antireflective layer reduces the reflectivity to the radiation that penetrates the photoresist by 70% or more. The AAPA teaches

on page 1, lines 23 – 24 and page 2, lines 1 – 6 wherein an antireflective layer reduces the reflectivity to a radiation that penetrates a photoresist by 70% or more. It would have been obvious to use the antireflective layer of the AAPA in the method of Takahashi and Bencher in order to substantially reduce standing waves as stated by the AAPA on page 1, lines 23 – 24 and page 2, lines 1 – 6.

With regard to claim 73, the AAPA teaches on page 1, lines 23 – 24 and page 2, lines 1 – 6 wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates the photoresist by 71%.

12. Claims 78 and 79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kayanuma, and Bencher as applied to claim 26 above, and further in view of the applicant's admitted prior art (AAPA).

With regard to claim 78, Kayanuma, and Bencher teach forming a photoresist over at least a portion of the anti-reflective layer. Kayanuma, and Bencher teach irradiating the photoresist. It is not clear if Takahashi and Bencher teach wherein the antireflective layer reduces the reflectivity to the radiation that penetrates the photoresist by 70% or more. The AAPA teaches on page 1, lines 23 – 24 and page 2, lines 1 – 6 wherein an antireflective layer reduces the reflectivity to a radiation that penetrates a photoresist by 70% or more. It would have been obvious to use the antireflective layer of the AAPA in the method of Kayanuma, and Bencher in order to substantially reduce standing waves as stated by the AAPA on page 1, lines 23 – 24 and page 2, lines 1 – 6. Kayanuma teaches in figure 4d and 4e wherein the subsequently

removing a portion of the exposed portion of the dielectric layer and a portion of the bottom electrode layer comprises performing an etch using the photoresist.

With regard to claim 79, the AAPA teaches on page 1, lines 23 – 24 and page 2, lines 1 – 6 wherein the anti-reflective layer reduces the reflectivity to the radiation that penetrates the photoresist by 71%.

13. Claims 88 and 94 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kayanuma and Bencher as applied to claims 86, 91, and 93 above, and further in view of AAPA.

Kayanuma and Bencher teach wherein said first and second fabrication processes are for CMOS processes. Kayanuma and Bencher do not teach that said first and second fabrication processes are for CMOS processes on a scale of 0.35μm or less. The AAPA teaches on page 1, lines 14 – 23 and page 3, lines 26 – 28 wherein first and second fabrication processes are for CMOS processes on a scale of 0.35μm or less. It would have been obvious to one of ordinary skill in the art to use the 0.35μm or less dimension of the AAPA in Kayanuma and Bencher in order to form more devices per unit area thus increasing the speed and the performance of the semiconductor chip.

14. Claims 90 and 96 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kayanuma and Bencher as applied to claims 86 and 91 above, and further in view of one of ordinary skill in the art (OOSA).

Kayanuma and Bencher teach wherein the second fabrication process forms a capacitor structure. It is not clear if the capacitor structure of Kayanuma and Bencher has a leakage

current between the top electrode from the conductive layer of not greater than $4fA/\mu m^2$. It is well known in the art to have a leakage current of not greater than $4fA/\mu m^2$. It would have been obvious to one of ordinary skill in the art to have a leakage current of not greater than $4fA/\mu m^2$ in the method of Kayanuma and Bencher in order to improve the properties and reliability of the resulting semiconductor device.

15. Claim 99 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi and Bencher as applied to claim 97 above, and further in view of AAPA.

With regard to claim 99, Takahashi and Bencher teach wherein said first and second fabrication processes are for CMOS processes. Takahashi and Bencher do not teach that said first and second fabrication processes are for CMOS processes on a scale of 0.35μm or less. The AAPA teaches on page 1, lines 14 – 23 and page 3, lines 26 – 28 wherein first and second fabrication processes are for CMOS processes on a scale of 0.35μm or less. It would have been obvious to one of ordinary skill in the art to use the 0.35μm or less dimension of the AAPA in Takahashi and Bencher in order to form more devices per unit area thus increasing the speed and the performance of the semiconductor chip.

16. Claim 101 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi and Bencher as applied to claim 97 above, and further in view of one of ordinary skill in the art (OOSA).

With regard to claim 101, Takahashi and Bencher teach wherein the second fabrication process forms a capacitor structure. It is not clear if the capacitor structure of Takahashi and

Bencher has a leakage current between the top electrode from the conductive layer of not greater than $4fA/\mu m^2$. It is well known in the art to have a leakage current of not greater than $4fA/\mu m^2$. It would have been obvious to one of ordinary skill in the art to have a leakage current of not greater than $4fA/\mu m^2$ in the method of Takahashi and Bencher in order to improve the properties and reliability of the resulting semiconductor device.

Response to Arguments

17. Applicant's arguments filed June, 30, 2003 have been fully considered but they are not persuasive.

18. With regard to the applicant's argument for claims 81 – 85 that "the comments of the Office Action with respect to this rejection are mixing up the order in which the various parameters defining the process are determined with the order in which the steps processes are executed," it should be noted that the rejections with regard to claims 81 – 85 are a direct result of the specification not enabling or disclosing steps to define optimized parameters for the process steps. While the process steps are defined in the specification no method to optimize them are defined. Therefore, the applicant's arguments are not persuasive, and the rejection is proper.

19. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., "inter-plate undercutting") are not recited in the rejected claim(s). Although the claims are interpreted in

light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Therefore, the applicant's arguments are not persuasive, and the rejection is proper.

20. With regard to the applicant's arguments that "inter-plate undercutting" is defined in the claims by "wherein a portion of the dielectric is removed from an intermediate region between the top electrode and the bottom electrode layer," it should be noted that this is a broad limitation which is read on by the art of record. This limitation specifically reads on portions of the dielectric layer removed from an area diagonally between the top electrode and the bottom electrode. Nothing in this limitation limits the claim to only an undercut between the electrodes. Therefore, the applicant's arguments are not persuasive, and the rejection is proper.

21. With regard to the applicant's argument that "Figure 4D of Kayanuma et al. clearly shows that the bottom electrode 52 is exposed when the top electrode 54 is formed," it should be noted that the rejection has been clarified to recite figure 4b of Kayanuma for showing "removing a portion of said tope electrode layer to expose a portion of the dielectric layer thereby forming a top electrode, wherein the bottom electrode layer is not exposed. Therefore, the applicant's arguments are not persuasive, and the rejection is proper.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E Brock II whose telephone number is (703)308-6236. The examiner can normally be reached on 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703)308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

Paul E Brock II
August 12, 2003